WHAT IS CLAIMED IS:

1. An apparatus for filtering a phase error signal, comprising:

a first filter subcircuit receiving a phase error signal from a phase comparator and filtering the error signal with the first filter subcircuit when enabled;

a second filter subcircuit receiving the phase error signal from the phase comparator and filtering the error signal with the second filter subcircuit when enabled; and

a first enable switch and a second enable switch which are activated in combination to control filtering of the error signal;

wherein the first filter subcircuit is enabled by activating a first combination of the first and second enable switches and the second filter subcircuit is enabled by activating a second combination of the first and second enable switches.

2. The apparatus of claim 1, wherein the second filter subcircuit has a higher bandwidth than the first filter subcircuit and the second filter subcircuit is momentarily activated to fast acquisition with the first filter subcircuit.

3. The apparatus of claim 1, further comprising a fast acquisition subcircuit including a fast acquisition enable switch and wherein fast acquisition of one of the first and second filter subcircuits is enabled when the fast acquisition switch is activated.

4. The apparatus of claim 3, wherein the fast acquisition subcircuit is temporarily enabled to underdampen the filtering.

5. The apparatus of claim 3, wherein the fast acquisition subcircuit comprises a fast acquisition resistor which is placed in parallel connection with a first resistor of one of the first and second filter subcircuits when the fast acquisition switch is activated.

6. The apparatus of claim 5, wherein the fast acquisition resistor comprises a resistance of approximately R1' determined by $R1'=\frac{R1}{\sqrt{F}-1}$, where R1 comprises the first resistor of the one of the first and second filter subcircuits and F comprises a fast acquisition factor.

7. The apparatus of claim 5, wherein the one of the first and second filter subcircuits further comprises a second resistor in series connection with the first resistor.

8. The apparatus of claim 7, wherein the fast acquisition resistor comprises a resistance of approximately R1' determined by $R1'=\frac{R1''\left[R''-R1(\sqrt{F}-1)\right]}{(R1''+R1)(\sqrt{F}-1)}$, where R1 comprises the first resistor and R1" comprises the second resistor of the one of the first and second filter subcircuits and F comprises a fast acquisition factor.

9. The apparatus of claim 7, wherein the fast acquisition resistor comprises a resistance of approximately R1' determined by $R1'=\frac{R1+R1''}{\sqrt{F}-1}$, where R1 comprises

the first resistor and R1" comprises the second resistor of the one of the first and second filter subcircuits and F comprises a fast acquisition factor.

10. The apparatus of claim 1, wherein the first filter subcircuit and the second filter subcircuit share common filter circuit elements.

11. The apparatus of claim 10, wherein the shared common filter circuit elements are a first capacitor and a first resistor in series both connected in parallel to a second capacitor.

12. The apparatus of claim 10, wherein the first filter subcircuit comprises filter circuit elements that are a subset of filter circuit elements of the second filter subcircuit.

13. The apparatus of claim 10, wherein the first combination comprises activating the first enable switch and deactivating the second enable switch to place a first capacitor in series connection with a first resistor and both the first capacitor and first resistor in parallel connection with second capacitor.

14. The apparatus of claim 10, wherein the second combination comprises deactivating the first enable switch and activating the second enable switch which places a first and a third capacitor in parallel connection and the first and third capacitor both in series connection with a first resistor and the first and third capacitor and the first resistor are all placed in parallel connection with a second and a fourth capacitor in series connection.

15. The apparatus of claim 10, wherein the first combination comprises activating both the first enable switch and the second enable switch to place a first capacitor in series connection with a first resistor and both the first capacitor and first resistor in parallel connection with a second capacitor.

16. The apparatus of claim 10, wherein the second combination comprises deactivating both the first enable switch and the second enable switch to place a first and a third capacitor and a first resistor all in series connection and all in parallel connection with a second and a fourth capacitor in series connection.

17. The apparatus of claim 1, wherein the first and the second enable switches are field effect transistors.

18. The apparatus of claim 1, wherein when the first enable switch is activated the first filter subcircuit is alternately referenced to a ground and a common cathode voltage selectable by a reference switch.

19. The apparatus of claim 1, wherein when the second enable switch is activated the second filter subcircuit is alternately referenced to a ground and a common cathode voltage selectable by a reference switch.

20. The apparatus of claim 1, wherein the first and second filter subcircuits each comprise a resistor-capacitor filter including a first capacitor and a first resistor in series both connected in parallel to a second capacitor.

21. The apparatus of claim 1, wherein the first and second filter subcircuits are implemented on a single integrated circuit.

22. The apparatus of claim 21, wherein the first and second enable switches are external to the integrated circuit.

23. The apparatus of claim 21, wherein the first and second enable switches are internal to the integrated circuit.

24. An apparatus for filtering a phase error signal, comprising:

a first filter subcircuit means for receiving a phase error signal from a phase comparator and filtering the error signal with the first filter subcircuit when enabled;

a second filter subcircuit means for receiving the phase error signal from the phase comparator and filtering the error signal with the second filter subcircuit when enabled; and

a first enable switching means and a second enable switching means for activating in combination to control filtering of the error signal;

wherein the first filter subcircuit is enabled by activating a first combination of the first and second enable switches and the second filter subcircuit is enabled by activating a second combination of the first and second enable switches.

25. The apparatus of claim 24, wherein the second filter subcircuit means has a higher bandwidth than the first filter subcircuit means and the second filter subcircuit means is momentarily activated to fast acquisition with the first filter subcircuit means.

26. The apparatus of claim 24, further comprising a fast acquisition subcircuit means for fast acquisition one of the first and second filter subcircuits when a fast acquisition switching means for enabling the fast acquisition subcircuit means is activated.

27. The apparatus of claim 26, wherein the fast acquisition subcircuit means is temporarily enabled to underdampen the filtering.

28. The apparatus of claim 26, wherein the fast acquisition subcircuit means comprises a fast acquisition resistor which is placed in parallel connection with a first resistor of one of the first and second filter subcircuit means when the fast acquisition switch is activated.

29. The apparatus of claim 28, wherein the fast acquisition resistor comprises a resistance of approximately R1' determined by $R1'=\frac{R1}{\sqrt{F}-1}$, where R1 comprises the first resistor of the one of the first and second filter subcircuit means and F comprises a fast acquisition factor.

30. The apparatus of claim 28, wherein the one of the first and second filter subcircuit means further comprises a second resistor in series connection with the first resistor.

31. The apparatus of claim 30, wherein the fast acquisition resistor comprises a resistance of approximately R1' determined by $R1'=\frac{R1''\left[R''-R1(\sqrt{F}-1)\right]}{(R1''+R1)(\sqrt{F}-1)}$, where R1 comprises the first resistor and R1" comprises the second resistor of the one of the first and second filter subcircuit means and F comprises a fast acquisition factor.

32. The apparatus of claim 30, wherein the fast acquisition resistor comprises a resistance of approximately R1' determined by $R1'=\frac{R1+R1''}{\sqrt{F}-1}$, where R1 comprises the first resistor and R1" comprises the second resistor of the one of the first and second filter subcircuit means and F comprises a fast acquisition factor.

33. The apparatus of claim 24, wherein the first filter subcircuit means and the second filter subcircuit means share common filter circuit elements.

34. The apparatus of claim 33, wherein the shared common filter circuit elements are a first capacitor and a first resistor connected in series both the first capacitor and first resistor connected in parallel to a second capacitor.

35. The apparatus of claim 33, wherein the first filter subcircuit means comprises filter circuit elements that are a subset of filter circuit elements of the second filter subcircuit means.

36. The apparatus of claim 33, wherein the first combination comprises activating the first enable switching means and deactivating the second enable switching means which places a first capacitor in series connection with a first resistor both in parallel connection with second capacitor.

37. The apparatus of claim 33, wherein the second combination comprises deactivating the first enable switching means and activating the second enable switching means which places a first and third capacitor in parallel connection, both in series connection with a first resistor and the first and third capacitor and first resistor are all placed in parallel connection with a second and fourth capacitor in series connection.

38. The apparatus of claim 33, wherein the first combination comprises activating the both the first enable switching means and the second enable switching means which places a first capacitor in series connection with a first resistor both in parallel connection with second capacitor.

39. The apparatus of claim 33, wherein the second combination comprises deactivating both the first enable switching means and the second enable switching means which places a first and third capacitor and a first resistor all in series connection, all placed in parallel connection with a second and fourth capacitor in series connection.

40. The apparatus of claim 24, wherein the first and second enable switching means are field effect transistors.

41. The apparatus of claim 24, wherein when the first enable switching means is activated, the first filter subcircuit means is alternately referenced to a ground and a common cathode voltage selectable by a reference switching means.

42. The apparatus of claim 24, wherein when the second enable switching means is activated the second filter subcircuit means is alternately referenced to a ground and a common cathode voltage selectable by a reference switching means.

43. The apparatus of claim 24, wherein the first and second filter subcircuit means each comprise a resistor-capacitor filter including a first capacitor and a first resistor in series both connected in parallel to a second capacitor.

44. The apparatus of claim 24, wherein the first and second filter subcircuit means are implemented on a single integrated circuit.

45. The apparatus of claim 44, wherein the first and second enable switching means are external to the integrated circuit.

46. The apparatus of claim 44, wherein the first and second enable switching means are internal to the integrated circuit.

47. A method of filtering a phase error signal in a phase lock loop, comprising the steps of:

receiving a phase error signal from a phase comparator;

filtering the error signal with a first filter subcircuit when the first filter subcircuit is enabled; and

filtering the error signal with a second filter subcircuit when the second filter subcircuit is enabled; and

controlling filtering of the error signal by activating a first enable switch and a second enable switch in combination, wherein the first filter subcircuit is enabled by activating a first combination of the first and second enable switches and the second filter subcircuit is enabled by activating a second combination of the first and second enable switches.

48. The method of claim 47, further comprising momentarily activating the second filter subcircuit to fast acquisition with the first filter subcircuit wherein the second filter subcircuit has a higher bandwidth than the first filter subcircuit.

49. The method of claim 47, further comprising fast acquisition of one of the first and second filter subcircuits with a fast acquisition subcircuit when a fast acquisition switch is activated.

50. The method of claim 49, wherein the fast acquisition subcircuit comprises temporarily enabling the fast acquisition subcircuit to underdampen the filtering.

51. The method of claim 49, wherein the fast acquisition subcircuit comprises a fast acquisition resistor which is placed in parallel connection with a first resistor of one of the first and second filter subcircuits when the fast acquisition switch is activated.

52. The method of claim 51, wherein the fast acquisition resistor comprises a resistance of approximately R1' determined by $R1'=\frac{R1}{\sqrt{F}-1}$, where R1 comprises the first resistor of the one of the first and second filter subcircuits and F comprises a fast acquisition factor.

53. The method of claim 51, wherein the one of the first and second filter subcircuits further comprises a second resistor in series connection with the first resistor.

54. The method of claim 53, wherein the fast acquisition resistor comprises a resistance of approximately R1' determined by $R1'=\frac{R1''\left[R''-R1(\sqrt{F}-1)\right]}{(R1''+R1)(\sqrt{F}-1)}$, where R1 comprises the first resistor and R1" comprises the second resistor of the one of the first and second filter subcircuits and F comprises a fast acquisition factor.

55. The method of claim 53, wherein the fast acquisition resistor comprises a resistance of approximately R1' determined by $R1'=\frac{R1+R1''}{\sqrt{F}-1}$, where R1 comprises the first resistor and R1" comprises the second resistor of the one of the first and second filter subcircuit means and F comprises a fast acquisition factor.

56. The method of claim 47, wherein the first filter subcircuit and the second filter subcircuit share common circuit elements.

57. The method of claim 56, wherein the shared common circuit elements are a first capacitor and a first resistor in series both connected in parallel to a second capacitor.

58. The method of claim 56, wherein the first filter subcircuit comprises filter circuit elements that are a subset of filter circuit elements of the second filter subcircuit.

59. The method of claim 56, wherein the first combination comprises activating the first enable switch and deactivating the second enable switch which places a first capacitor in series connection with a first resistor both in parallel connection with second capacitor.

60. The method of claim 56, wherein the second combination comprises deactivating the first enable switch and activating the second enable switch which places a first and third capacitor in parallel connection, both in series connection with a first resistor and the first and third capacitor and first resistor are all placed in parallel connection with a second and fourth capacitor in series connection.

61. The method of claim 56, wherein the first combination comprises activating the both the first enable switch and the second enable switch which places a first capacitor in series connection with a first resistor both in parallel connection with second capacitor.

62. The method of claim 56, wherein the second combination comprises deactivating both the first enable switch and the second enable switch which places a first and third capacitor and a first resistor all in series connection, all placed in parallel connection with a second and fourth capacitor in series connection.

63. The method of claim 47, wherein the first and second enable switches are field effect transistors.

64. The method of claim 47, wherein when the first enable switch is activated the first filter subcircuit is alternately referenced to a ground and a common cathode voltage selectable by a reference switch.

65. The method of claim 47, wherein when the second enable switch is activated the second filter subcircuit is alternately referenced to a ground and a common cathode voltage selectable by a reference switch.

66. The method of claim 47, wherein the first and second filter subcircuits each comprise a resistor-capacitor filter including a first capacitor and a first resistor in series both connected in parallel to a second capacitor.

67. The method of claim 47, wherein the first and second filter subcircuits are implemented on a single integrated circuit.

68. The method of claim 67, wherein the first and second enable switches are external to the integrated circuit.

69. The method of claim 67, wherein the first and second enable switches are internal to the integrated circuit.